CLAIMS:

1. A metallization structure in a multilayer stack, which is arranged at a distance from a ground electrode, characterized in that the metallization structure has a capacitor electrode (22) and a line (24) that acts as a coil, where the capacitor electrode (22) and the line (24) are arranged in a common plane which lies parallel to the ground electrode (30) at a distance $h_1$, and in that

$$\frac{w}{h_1} > 3,$$

where w is the width of the line (24).

2. A metallization structure as claimed in claim 1, characterized in that a second ground electrode (32) is provided, the plane comprising capacitor electrode (22) and line (24) being arranged parallel to said second ground electrode at a distance $h_2$, and in that the plane comprising capacitor electrode (22) and line (24) lies between the first and second ground electrodes (30, 32), where

$$\frac{w}{h_2} > 3.$$

3. A multilayer stack comprising a metallization structure as claimed in claim 1 or 2, characterized in that the metallization structure (20) is arranged on a dielectric layer (14), the dielectric constant ($\varepsilon_{medium}$) of which is greater than the dielectric constant ($\varepsilon$) of surrounding dielectric layers (12, 16).

4. A multilayer stack as claimed in claim 3, characterized in that the following applies in respect of the dielectric constant ($\varepsilon_{medium}$) of the dielectric layer (14):

$\varepsilon < \varepsilon_{medium}$.

5. A multilayer stack as claimed in claim 3 or 4, characterized in that the following applies in respect of the layer thickness ($d_{medium}$) of the dielectric layer (14):

$$\frac{\varepsilon_{medium} \cdot d_{\varepsilon}}{\varepsilon \cdot d_{medium}} > 5.$$

6. A multilayer stack as claimed in claim 3 or 4, characterized in that

$$\frac{\varepsilon_{medium} \cdot d_{\min}}{d_{medium} \cdot \varepsilon} > 7,$$

where $d_{min}$ is the minimum distance to the next metallization structure in the plane.

7. A multilayer stack as claimed in claim 3, characterized in that it comprises magnetic layers.

8. A multilayer stack as claimed in any of claims 3 to 7, produced in a multilayer laminate process.

9. A multilayer stack as claimed in any of claims 3 to 7, produced in an LTCC process.

10. An electrical module which comprises the metallization structure as claimed in claim 1 or 2, or a multilayer stack as claimed in any of claims 3 to 7 for implementing a filter function for high frequency signals.